In the Drawings:

Please replace figures 3 and 15 in their entirety with the replacement figures 3 and 15 in compliance with 37 C.F.R. 1.84(p)(5) provided herewith.

In the Specification:

Please amend Paragraph numbers 74 as follows (the changes on these paragraphs are shown with ~~strikethrough~~ for deleted matter and underlines for added matter):

[0074] The DPSSRAM blocks 216A, 216B are also coupled with the daughter card 204 via the DPSSRAM daughter card interfaces 232A, 232B. In one embodiment, the DPSSRAM daughter card interface 232A, 232B are each at least 64 bits wide and operate at a frequency of at least 50 MHz. The SRAM control logic ~~328A, 328B228A, 228B~~ 228A, 228B, 328 is coupled with the daughter card 204 via SRAM control logic daughter card interfaces 234A, 234B. In one embodiment, the SRAM control logic 228A, 228B, 328 is a custom designed device using a CMOS Programmable Logic Device ("CPLD"). Operation of the SRAM control logic 228A, 228B, 328 is described in more detail below.